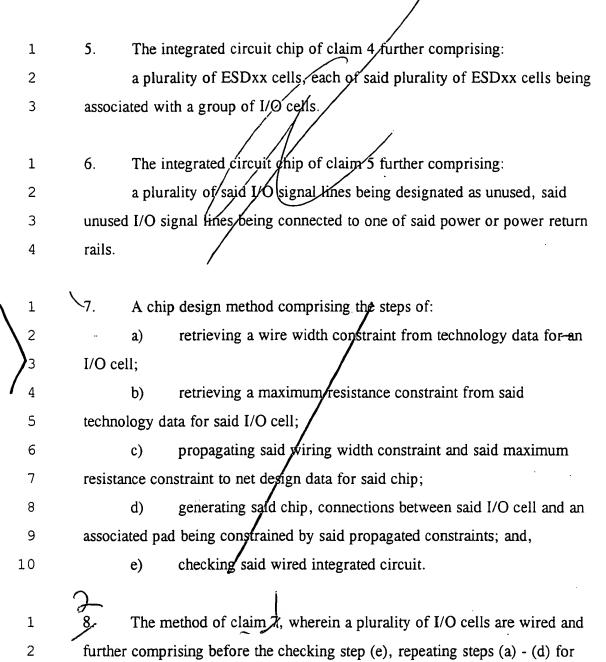
CLAIMS

We claim:

1	1. An integrated circuit chip comprising:
2	an array of pads, said pads including signal I/O, power and power
3	return pads;
4	a plurality of I/O cells each/being connected to one of said I/O pads by
5	I/O signal wiring in one or more wiring layers; and
6	a plurality of ESD protection devices, each of said plurality of ESD
7	protection devices being connected to one of said array of pads by a metal
8	line, said metal line meeting an ESD width constraint and having a resistance
9	below an ESD resistance constraint.
	/ /:
1	2. The integrated circuit chip of Claim 1, wherein the plurality of ESD
2	protection devices comprises.
3	an ESD protect device in each of said plurality of I/O cells connected
4	between an I/O circuit/in said I/O cell and one of said I/O signal pads.
1 .	3. The integrated circuit of claim 2 wherein each said ESD protect device
2	is further connected to power rails and power return rails connected to said
3	circuit.
1	4. The integrated circuit chip of claim 3, wherein the plurality of ESD
2	protection devices comprises:
3	an ESP xx cell connected between power rails and power return rails
4	for at least two different power supplies.





each of said plurality of I/O cells.

3

	Ŧ	9. The method of claim 8, further comprising before the checking step			
	2	(e), the step of:			
\	3	d1) wiring any unused chip pads to a cell including a connection to			
/	4	power rail or to a power return rail.			
Br.)				
sys Br	1	10. The method of claim 8, further comprising before the checking step			
? /	2	(e), the step of:			
- 1	3	d1) wiring any unused chip pads to a cell including an ESD protect			
·	4	device.			
	1	The method of claim 8, wherein the generating step (d) comprises the			
	2	step of:			
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	4	width and maximum resistance constraints; and			
	5	ii) routing a connection between each said placed I/O cell and its			
	6	said associated pad, each said routed connection meeting said propagated wire			
	7	width and maximum resistance constraints.			
1 1. 1. 1 1 1 10	1	12. The method of claim 11, wherein the checking step (e) comprises			
: <u>- </u>	2	checking connections made in said generating step (d) against propagated wire			
	3	width and maximum resistance constraints.			
	1	13. A chip design method comprising the steps of:			
	2	a) / retrieving a power route pattern instruction;			
	3	by identifying power and power return connections:			

connecting each said placed ESDxx cell between power rails

and power return rails for at least two different power supplies; and,

7

8

d)



e)	checking	said	wired	integrated	circuit

- 18. A system for integrated circuit chip design comprising:
 means for retrieving net constraints from technology data;
 means for placing a plurality of I/O cells; and
 means for connecting each of said placed I/O cells to I/O cells to an
 I/O pad according to said retrieved net constraints.
- 19. The system of claim 18, wherein said retrieved constrains include power bussing constraints, said system further comprising:

 means for routing power and power return connections according to said power bussing constraints.
- 20. The system of claim 18, further comprising:

 means for grouping I/O cells; and

 means for placing an ESDxx cell with each group of I/O cells.